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EXAMINER	
WASHBURN, DANIEL C	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/655,695	IOTOV, MIHAIL	
	Examiner	Art Unit	
	DANIEL WASHBURN	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5,9-12 and 16-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,9-12 and 16-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect the claims have been considered but are moot in view of the new ground(s) of rejection.

Method Claims Tied to another Statutory Category

The method claims are statutory as claim 1 recites at least, "displaying pointers to time points of interest on the displayed waveform portions" and "receiving edits to the time points of interest in response to a user moving the pointers on the interactive graphical user interface."

Claim Objections

Claim 5 is objected to because of the following informalities: Lines 2 and 3 of claim 5 read, "...of the first, **second. third**, and fourth waveforms..." The examiner assumes they should read, "...of the first, **second, third**, and fourth waveforms..."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 9-11, and 17-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 11 recite the limitation "the interactive graphical user interface" in lines 22 and 24, respectively. There is insufficient antecedent basis for this limitation in

the claims. For purposes of examination, the examiner assumes the claims should read, "an interactive graphical user interface."

Claims 9 and 10 recite the limitation "updating the timing parameters...further comprises..." in lines 2 and 3. There is insufficient antecedent basis for this limitation in the claims.

Claim 17 recites the limitations "the source multi-cycle edge" and "the destination multi-cycle edge" in lines 5 and 7, respectively. There is insufficient antecedent basis for these limitations in the claim.

Claims 18 and 19 recite the limitation "the new timing parameters" in line 4. There is insufficient antecedent basis for this limitation in the claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5, 11, 12, 16-19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamoto et al. (US 7,089,517) in view of Liu et al. (US 6,662,126), in view of Pramanick et al. (US 2004/0216005), and further in view of Beck et al. (US 6,624,829).

RE claims 1 and 11, Yamamoto describes a method and computer-readable medium encoded with a computer program, the computer program comprising a set of instructions for displaying and modifying timing data generated by an EDA tool used to

simulate a circuit being designed, wherein the set of instructions when executed by a computer causes the computer to:

receive the timing data from the EDA tool, the timing data including at least multiple periods of a clock signal (6:20-42 "The present invention proposes that the IC simulation model and initial simulation testbench is used together with electronic design automation (EDA) tools to design verification using event based test system" ... 6:65-7:27 "a design test station (DTS) 82 is an event based test system provided to test the function of the silicon prototype 63 using the test vectors produced based on the event data derived from a VCD (value change dump) file 59. The VCD file 59 is produced by executing the design verification 55 and simulation 56 on the initial design 54 with use of an initial testbench 58. Since the testbench 58 is created in the event format and the resultant VCD file 59 is also in the event format, the data in the VCD file 59 can be directly used in the event based test system 82 to test the design" ... 7:49-55 "In the foregoing embodiment of the present invention, the event format test vectors resulted from the testbench 58 are generated by the event based test system at a rate, for example, 10,000 times higher than a simulator. This is done by scaling the function of the event based test system in which an event clock and event timing data are multiplied by a predetermined factor"),

enable selection of the first clock signal from the plurality of signals based on an input received from a user (7:9-27 "The EDA tools such as simulation analysis/debug 85 and waveform editor/viewer 86 are linked to the design test station (DTS) 82." The

simulation analysis/debug 85 is considered to enable a user to select the clock signal from the plurality of signals);

generate a first waveform for the first selected clock signal using the timing data (7:9-27 "The EDA tools such as simulation analysis/debug 85 and waveform editor/viewer 86 are linked to the design test station (DTS) 82" ... "The event based test system 82 incorporates software tools for editing and viewing waveforms such as VCD waveform editor/viewer 87, event waveform editor/viewer 88 and DUT (device under test) waveform editor/viewer 89");

select for display a portion of the first waveform (7:9-27 "The EDA tools such as simulation analysis/debug 85 and waveform editor/viewer 86 are linked to the design test station (DTS) 82" ... "The event based test system 82 incorporates software tools for editing and viewing waveforms such as VCD waveform editor/viewer 87, event waveform editor/viewer 88 and DUT (device under test) waveform editor/viewer 89" Thus, at least a portion of the clock signal is displayed with the rest of the waveforms in a waveform editor/viewer);

display time points of interest on the displayed waveform portions (7:9-27 "The EDA tools such as simulation analysis/debug 85 and waveform editor/viewer 86 are linked to the design test station (DTS) 82" ... "The event based test system 82 incorporates software tools for editing and viewing waveforms such as VCD waveform editor/viewer 87, event waveform editor/viewer 88 and DUT (device under test) waveform editor/viewer 89" ... "In the event based test system, for example, an event may be inserted in a particular timing or an edge timing of an event may be changed

through the event waveform editor/viewer 88" Thus, the edges of events (e.g., either a 0 to 1 transition or a 1 to 0 transition) are considered displayed time points of interest);

receive edits to the time points of interest in response to a user moving the time points of interest on the interactive graphical user interface (7:24-27 "In the event based test system, for example, an event may be inserted in a particular timing or an edge timing of an event may be changed through the event waveform editor/viewer 88"); and

modify the circuit so as to cause a change in relative timing of the at least one edge based on edits to the time points of interest (7:28-8:4 "By executing the test vectors, the event based test system 82 produces a test result file 83 which is feedbacked to the EDA design environment and to the EDA tools through a testbench feedback 99" ... "Thus, when the silicon prototype 63 is connected to the event test system, the silicon prototype 63 is tested at very high speed. Since the data concerning the silicon prototype 63 is now copied in the event test system, the modification of test vectors and the resultant response or changes in the design can be conducted in the event test system at high speed. The test results and the modification of the test vectors are feedbacked to the EDA tools 85, 86 and the testbench 81. After these processes, final silicon fabrication is done at stage 91 to produce the final IC device 92 which will be tested in a production test stage 93").

Yamoto doesn't describe but Liu describes a system and method of measuring signal skew on a chip using on-chip sampling wherein the system includes components to

receive the timing data from the on chip-sampling, the timing data including at least multiple periods of a plurality of clock signals (3:11-37 "Thereafter, by analyzing the outputs from various on-chip samplers, the skew of the global on-chip signal between different points on the chip can be determined" ... "The on-chip sampler 100 is primarily used to detect transitions, i.e., rising and falling edges, of an on-chip signal. An externally generated reference signal, EXT, and the on-chip signal, CHIP_CLK, serve as inputs to the on-chip sampler 100." Thus, EXT (or MOD_EXT) and CHIP_CLK are collectively considered timing data including at least multiple periods of a plurality of clock signals (Figure 5a and 4:61-65 describes the multiple periods of the plurality of clock signals)),

enable selection of first and second clock signals from the plurality of signals based on an input received from a user (3:10-37 "Thereafter, by analyzing the outputs from various on-chip samplers, the skew of the global on-chip signal between different points on the chip can be determined." Thus, a user can select which on-chip sampler output to analyze);

generate a first waveform for the first selected clock signal and a second waveform for the second selected clock signal using the timing data (Figure 5a and 4:61-65 describes the waveform outputs that are generated by the first and second clock signals at a particular on-chip sampler);

generate a third waveform characterized as being a delayed replica of the first waveform and having transitions (Figure 6 and 7:61-8:22 describes MOD_EXT_2, which is a delayed replica of MOD_EXT_1);

generate a fourth waveform characterized as being a delayed replica of the second waveform and having transitions (Figure 6 and 7:61-8:22 describes CHIP_CLK_2, which is a delayed replica of CHIP_CLK_1);

select for display a portion of each of the first, second, third, and fourth waveforms (Figure 6 illustrates that the four waveforms are all presented to a user in order to allow the user to determine the amount of signal skew present on the chip).

All the above-described elements of claims 1 and 11 are known in Yamoto in view of Liu, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Yamoto the system and method of receiving timing data, wherein the timing data includes at least multiple periods of a plurality of clock signals, enabling selection of first and second clock signals from the plurality of signals based on an input received from a user, generating a first waveform for the first selected clock signal and a second waveform for the second selected clock signal using the timing data, generating a third waveform characterized as being a delayed replica of the first waveform and having transitions, generating a fourth waveform characterized as being a delayed replica of the second waveform and having transitions, and selecting for display a portion of each of the first, second, third, and fourth waveforms, as taught by Liu, and displaying these measured waveforms on the interactive graphical user interface described by Yamoto, in order to allow a user to measure the signal skew occurring on the silicon prototype and make precise changes to the timing diagrams

based on the measured signal skew, which allows a user to correct any timing errors occurring on the silicon prototype faster and more accurately, as the user can factor in the amount of signal skew that exists on the silicon prototype when making timing adjustments.

Yamoto in view of Liu doesn't describe but Pramanick describes a system that is able to

generate a waveform having transitions defining at least one launch edge (Figures 4B and 5A-5C and paragraphs 0043-0046 describe two flip-flops and their associated timing diagrams. Figure 5A illustrates that the input of the first flip-flop is driven high at 61, then at clk2 the input is latched into the first flip-flop (signal b at arrow 62), there is a bit of a propagation delay due to gate logic between the two flip-flops, and then the signal shows up at the input to the second flip-flop (signal c) and it is latched into the second flip-flop at clk3 (arrow 64 and signal d). Signal b at arrow 62 is considered the launch edge of the first clock signal at which the first storage element releases a data signal);

generate a waveform having transitions defining at least one latch edge (Figures 4B and 5A-5C and paragraphs 0043-0046 describe two flip-flops and their associated timing diagrams. Figure 5A illustrates that the input of the first flip-flop is driven high at 61, then at clk2 the input is latched into the first flip-flop (signal b at arrow 62), there is a bit of a propagation delay due to gate logic between the two flip-flops, and then the signal shows up at the input to the second flip-flop (signal c) and it is latched into the second flip-flop at clk3 (arrow 64 and signal d). Signal d at arrow 64 is considered the

latch edge of the second clock signal at which the second storage element captures the data signal);

select for display a portion of each of the waveforms, the displayed portion of a first waveform comprising the at least one launch edge and the displayed portion of a second waveform comprising the at least one latch edge (Figures 4B and 5A-5C and paragraphs 0043-0046 describe two flip-flops and their associated timing diagrams. Figure 5A illustrates that the input of the first flip-flop is driven high at 61, then at clk2 the input is latched into the first flip-flop (signal b at arrow 62), there is a bit of a propagation delay due to gate logic between the two flip-flops, and then the signal shows up at the input to the second flip-flop (signal c) and it is latched into the second flip-flop at clk3 (arrow 64 and signal d). These waveforms are presented to the user using the system described in Figure 6 (see 0048-0053));

and modify the circuit so as to cause a change in relative timing of the at least one launch edge and the at least one latch edge based on edits to the time points of interest (0043-0047 and Figures 5A-5C describe "In Fig. 5B, suppose that due to a certain reason, the propagation delay deltabc2 through the random logic 52 is significantly larger than the normal propagation delay deltabc1 of Fig. 5A. Due to this large delay, the value at the input "c" of the flip-flop 53...shows an incorrect value" ... "The cause of this failure is the excessive delay through the random logic 52 for the signal to propagate from the input "b" to the output "c"...In Figure 5C, if an extra time 66a and 66b is added between the clock clk2 and clock clk3, the value of the input "c" of the flip-flop 53 changes to "1" with the rising edge of the clock clk3, which shows the

correct value." Thus, the circuit has been modified so as to cause a change in relative timing of the at least one launch edge and the at least one latch edge based on edits to the time points of interest).

All the above-described elements of claims 1 and 11 are known in Yamoto, Liu, and Pramanick, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Yamoto, and Liu the system and method wherein the system is able to generate a waveform having transitions defining at least one launch edge; generate a waveform having transitions defining at least one latch edge; select for display a portion of each of the waveforms, the displayed portion of a first waveform comprising the at least one launch edge and the displayed portion of a second waveform comprising the at least one latch edge; and modify the circuit so as to cause a change in relative timing of the at least one launch edge and the at least one latch edge based on edits to the time points of interest, as taught by Pramanick, as displaying this particular circuit behavior doesn't change the operation of the system, and it could be used to achieve the predictable result of determining if the data being passed from one flip-flop to the next flip-flop has been on the data line long enough to allow the signal to reach the receiving flip-flop and stabilize before the receiving flip-flop attempts to latch it in. The advantage of this test is it allows a user to evaluate the integrity of each data signal as it is input into the receiving circuit module.

Yamoto in view of Liu and further in view of Pramanick doesn't describe but Beck describes a system that is able to

receive edits to the time points of interest in response to a user moving the pointers on the interactive graphical user interface (Figures 15A and 15P and 47:53-48:41 describe sequence labels 15110-A through C, which are considered pointers on the interactive graphical user interface. "a user 101 may click on sequence label 15110-C and select a delete option button in the dialogue box. In response to this action, display coordinator 630 deletes line 15114 and shifts workspace intervals 15116, and the waveforms contained therein, to the space formerly occupied by workspace interval 15118. If user 101 clicks on sequence label 15110-B, the dialogue box provides an option so that user 101 may indicate whether it is desired that workspace interval 15116 be shifted to the right or that workspace interval 15118 be shifted to the left. In the illustrated embodiment, when a constant-time line is deleted, all pulsed or busses are deleted that span across two or more constant-time lines that include the deleted one." Thus, when a user edits the sequence labels corresponding to the constant-time lines (considered pointers) the user is also editing the time points of interest on the waveform diagram).

All the elements of claims 1 and 11 are known in Yamoto, Liu, Pramanick, and Beck, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Yamoto, Liu, and Pramanick the system and method wherein

the system is able to receive edits to the time points of interest in response to a user moving the pointers on the interactive graphical user interface, as taught by Beck, as this doesn't change the overall operation of the system disclosed in Yamoto, Liu, and Pramanick, and it could be used to achieve the predictable result of allowing a user to edit all the waveforms corresponding to a particular time interval, which allows a user to easily implement or remove a timing delay throughout the system, which is helpful at least when debugging timing problems.

RE claim 5, Yamoto doesn't describe but Liu describes the method of claim 1, wherein:

the time duration of the display of the first, second, third and fourth waveforms in a window of the interactive graphical user interface is a time period selected to be a multiple of the least common multiple of periods of the first clock signal and the second clock signal (Figure 6 illustrates that the display of the first, second, third and fourth waveforms in a window of the interactive graphical user interface is a time period selected to be a multiple of the least common multiple of periods of the first clock signal and the second clock signal). See the rejection of claims 1 and 11 for rationale.

RE claim 12, Yamoto doesn't describe but Liu describes the computer-readable medium according to claim 11 wherein:

the display of the portion of each of the waveforms in the interactive graphical user interface further comprises display of each of the portions of the waveforms in synchronism (Figure 6 illustrates display of each of the portions of the waveforms in synchronism). See the rejection of claims 1 and 11 for rationale.

RE claim 16, Yamoto in view of Liu doesn't describe but Pramanick describes the computer-readable medium according to claim 11 wherein the display of the pointers to the time points of interest on the waveforms further comprises:

display of a launch edge of the third waveform that triggers a first latch to capture a data signal (0043-0047 and Figs. 5A-5C describe signal a, which is a launch edge of a third waveform that triggers a first latch to capture a data signal (data is captured when signal b goes high); and

display of a latch edge of the fourth waveform that triggers a second latch to capture the data signal (0043-0047 and Figs. 5A-5C describe signal d, which is a latch edge of a fourth waveform that triggers a second latch to capture the data signal).

Further, Beck describes

display of a first pointer to an edge of the third waveform (Figures 15A and 15P and 47:53-48:41 describe sequence label 15110-A, which is considered a pointer to an edge of a waveform); and

display of a second pointer to an edge of the fourth waveform (Figures 15A and 15P and 47:53-48:41 describe sequence label 15110-B, which is considered a second pointer to an edge of a waveform).

All the elements of claim 16 are known in Yamoto, Liu, Pramanick, and Beck, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Yamoto in view of Liu a system that is able to display a first pointer to a launch edge of the third waveform that triggers a first latch to capture a data

signal; and display of a second pointer to a latch edge of the fourth waveform that triggers a second latch to capture the data signal, as suggested by Pramanick in view of Beck, as this doesn't change the overall operation of the system, and it could be used to achieve the predictable result of allowing a user to easily determine if the data being passed from one flip-flop to the next flip-flop has been on the data line long enough to allow the signal to stabilize before the receiving flip-flop attempts to latch it in. The advantage of this test is it allows a user to evaluate the integrity of each data signal as it is input into the receiving circuit module.

RE claim 17, Yamoto in view of Liu doesn't describe but Pramanick describes the computer-readable medium according to claim 16 wherein the display of the pointers to the time points of interest on the waveforms further comprises:

display of an edge of the first waveform that corresponds to the source multi-cycle edge of the first waveform (Figures 5A-C and 0043-0046 describe signal b, which is considered the source multi-cycle edge of the first waveform, see the rejection of claims 18 and 19 for a more complete discussion); and

display of an edge of the second waveform that corresponds to the destination multi-cycle edge of the second waveform (Figures 5A-C and 0043-0046 describe signal d, which is considered the destination multi-cycle edge of the first waveform, see the rejection of claims 18 and 19 for a more complete discussion).

Further, Beck describes

display of a third pointer to an edge of a first waveform (Figures 15A and 15P and 47:53-48:41 describe sequence labels 15110-A through C, and further describes

that more sequence labels may be added in order to add workspace intervals to the timing diagram. Sequence label 15110-C (labeled 'T' in Figure 15A) is considered a third pointer to an edge of the first waveform); and

display of a fourth pointer to an edge of the second waveform (Figures 15A and 15P and 47:53-48:41 describe sequence labels 15110-A through C, and further describes that more sequence labels may be added in order to add workspace intervals to the timing diagram. The at least one additional sequence label that may be added in order to add workspace intervals is considered a fourth pointer to an edge of the second waveform that corresponds to the destination multi-cycle edge of the second waveform).

All the elements of claim 17 are known in Yamoto, Liu, Pramanick, and Beck, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Yamoto and Liu the system and method wherein the display of the pointers to the time points of interest on the waveforms further comprises: display of a third pointer to an edge of the first waveform that corresponds to the source multi-cycle edge of the first waveform; and display of a fourth pointer to an edge of the second waveform that corresponds to the destination multi-cycle edge of the second waveform, as suggested by Pramanick in view of Beck, as this doesn't change the overall operation of the system and it could be used to achieve the predictable result of determining if the data being passed from one flip-flop to the next flip-flop has been on the data line long enough to allow the signal to stabilize before the receiving flip-flop

attempts to latch it in. The advantage of this test is it allows a user to evaluate the integrity of each data signal as it is input into the receiving circuit module.

As to claims 18 and 19, Yamoto in view of Liu doesn't describe a computer-readable medium wherein the set of instructions when executed by the computer further causes the computer to generate the new timing parameters based on the edits to the time points of interest by changing a multi-cycle value that represents a number of active edges in the first (second) clock signal from the launch edge to the latch edge in response to the user moving the first (second) or third (fourth) pointer on the interactive graphical user interface.

However, Pramanick describes a method wherein updating the timing parameters based on the edits to the time points of interest further comprises updating a multi-cycle value that represents a number of active edges in the first or second clock signal between the launch edge and the latch edge (Figures 5B and 5C and paragraphs 0044-0046 describe that a user is able to alter the timing of the clock (considered a second clock signal) that two flip-flops operate off of in order to correct a timing error. In Figure 5B the propagation delay (delta bc2) between the launch edge of a first flip-flop and the latch edge of a second flip-flop is so large that a clock cycle passes before the value is ready to be latched by the second flip-flop. The logic that takes place between these two flip-flop operations is considered to have a multi-cycle value of one, as there is one active (positive) edge in the clock signal between the launch edge and the latch edge. A problem occurs at this point because the second flip-flop attempts to latch the incoming value at clk3, but the value isn't ready, so the second flip-flop latches an

incorrect value. In order to remedy this problem a user is able to alter the timing parameters of the clock during the propagation delay in order increase the period of the clock. The increased clock period gives the launch edge from the first flip-flop enough time to propagate through the required logic and arrive at the input of the second flip-flop before the next positive edge of the clock, which corrects the timing error. The multi-cycle value that represents a number of active edges in the clock signal between the launch edge and the latch edge has been updated from one to zero, as now there are zero active edges in the clock between the launch edge and the latch edge).

Further, Beck describes a computer that generates new timing parameters based on edits to time points of interest in response to a user moving pointers on an interactive graphical user interface (Figures 15A and 15P and 47:53-48:41 describe sequence labels 15110-A through C, which are considered pointers to specific edges of waveforms. A user is able to move, add, or delete the sequence labels in order to alter the timing diagrams and generate new timing parameters).

All the elements of claims 18 and 19 are known in Yamoto, Liu, Pramanick, and Beck, the only difference is the combination of old elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in Yamoto in view of Liu the system and method wherein the computer generates the new timing parameters based on the edits to the time points of interest by changing a multi-cycle value that represents a number of active edges in the first (second) clock signal from the launch edge to the latch edge in response to the

user moving the first (second) or third (fourth) pointer on the interactive graphical user interface, as suggested by Pramanick in view of Beck, as this doesn't change the overall operation of the system, and it could be used to achieve the predictable result of determining if the data being passed from one flip-flop to the next flip-flop has been on the data line long enough to allow the signal to stabilize before the receiving flip-flop attempts to latch it in. The advantage of this test is it allows a user to evaluate the integrity of each data signal as it is input into the receiving circuit module.

RE claim 21, Yamoto describes the computer readable medium according to claim 11 wherein the set of instructions when executed by the computer further causes the computer to generate updated waveforms for the signals using updated timing data, wherein the EDA tool generates the updated timing data by compiling, simulating and performing verification analysis on the circuit design using the new timing parameters and displays the updated waveforms in the interactive graphical user interface (6:43-8:4 describes that a user updates the waveforms and the new timing parameters are passed to the EDA tools in order to modify the circuit design and run a new circuit simulation to determine if all incorrect operations have been rectified. The process is repeated until the circuit is functioning according to the user's requirements).

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamoto et al. (US 7,089,517) in view of Liu et al. (US 6,662,126), in view of Pramanick et al. (US 2004/0216005), and further in view of Beck et al. (US 6,624,829), as applied to claim 1 above, and further in view of Tojima et al. (US 6,898,771).

Concerning claims 9 and 10, the combination of Yamoto, Liu, Pramanick, and Beck doesn't describe a method wherein updating the timing parameters based on the edits to the time points of interest further comprises inverting the launch edge of the first clock signal, either in a design file or as an input to a static timing verification tool, nor does the combination describe a method wherein updating the timing parameters based on the edits to the time points of interest further comprises inverting the latch edge of the second clock signal.

However, Tojima describes a method wherein updating the timing parameters based on edits to the time points of interest further comprises inverting displayed waveforms, which is considered to include inverting the logic that controls the launch edge and latch edge for storage devices (Figures 13A and 13B and column 18 lines 20-51 describes that a user may double-click on a waveform in order to invert the entire signal). It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Yamoto, Liu, Pramanick, and Beck the method of inverting the launch edge of a clock signal and inverting the latch edge of a clock signal, as taught by Tojima, in order to test the performance of a circuit using negative logic, where the flip-flops launch and latch values based on the negative edges of a clock signal. The advantage of testing a circuit using negative logic is that a user can see how the circuit reacts to a wider range of tests, which helps create a more robust design.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamoto et al. (US 7,089,517), in view of Liu et al. (US 6,662,126), in view of Pramanick et al.

(US 2004/0216005), and further in view of Beck et al. (US 6,624,829), as applied to claim 11 above, and further in view of Chan (US 6,466,898).

The combination of Yamoto, Liu, Pramanick, and Beck doesn't describe a computer readable medium wherein the circuit design is a design for a field programmable gate array.

However, the background of Chan describes that a logic simulator is an essential electronic design automation (EDA) tool to facilitate the design and debug of very large scale integrated circuits (column 1 lines 5-20). The background of Chan further describes that some EDA vendors have hardware-accelerators or hardware emulators, where the hardware emulators program field programmable gate array (FPGA) chips (column 2 lines 4-23). It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Yamoto, Liu, Pramanick, and Beck the system of using the EDA tool and timing analyzer to program an FPGA, as taught by the background of Chan, in order to apply the system taught by Yamoto, Liu, Pramanick, and Beck to debugging and programming FPGA chips, which increases the market demand for the system, as an FPGA chip is a common and popular chip for commercial and educational purposes.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL WASHBURN whose telephone number is (571)272-5551. The examiner can normally be reached on Monday through Friday 8:30 a.m. to 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on (571) 272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dan Washburn/
Examiner, Art Unit 2628
11/18/08

/Ulka Chauhan/
Supervisory Patent Examiner, Art Unit 2628